NCV4276

Advance Information

Low-Drop Voltage Regulator

This industry standard linear regulator has the capability to drive loads up to 400 mA at 5.0 V, 3.3 V, 2.5 V and 1.8 V, and is also available in an adjustable version. Package options include DPAK, D^2PAK, and TO-220. This device is pin-for-pin compatible with the Infineon part number TLE4276.

Features

- 5.0 V, 3.3 V, 2.5 V, 1.8 V, or Adjustable, ±4%, 400 mA Output Voltage
- 500 mV (max) Dropout Voltage
- Inhibit Input
- Very Low Current Consumption
- Fault Protection
  - +45 V Peak Transient Voltage
  - -42 V Reverse Voltage
  - Short Circuit
  - Thermal Overload
- NCV Prefix for Automotive and Other Applications Requiring Site and Change Control

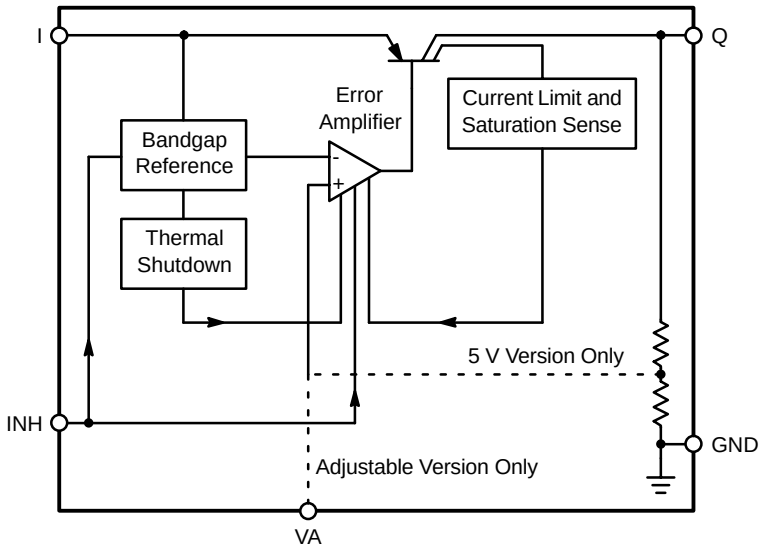

Figure 1. Block Diagram

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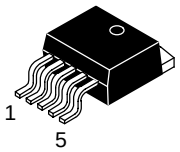
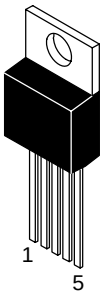


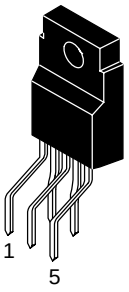
DPAK
5-PIN
DT SUFFIX
CASE TBD

D^2PAK
5-PIN
DP SUFFIX
CASE 936A-02

Pin 1. I
2. INH
3. GND
4. NC/VA
5. Q



TO-220
FIVE LEAD
TQ SUFFIX
CASE 314D



TO-220
FIVE LEAD
TQVA SUFFIX
CASE 314N

DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 5 of this data sheet.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS*†

Rating		Min	Max	Unit
Input [I (DC)]		-42	45	V
Input [I (Peak Transient Voltage)]		-	TBD	V
Inhibit INH		-42	45	V
Voltage Adjust Input VA		-0.3	10	V
Output (Q)		-1.0	40	V
Ground (GND)		-	100	mA
Operating Range (I)		Q + 0.5	40	V
Operating Range (I), Adjustable Device, Q < 4.0 V		4.5	40	V
ESD Susceptibility (Human Body Model)		2.0	-	kV
Junction Temperature		-40	150	°C
Storage Temperature		-50	150	°C
Package Thermal Resistance, DPAK, 5-Pin :	Junction-to-Case, $R_{\theta JC}$ Junction-to-Ambient, $R_{\theta JA}$	- -	TBD TBD	°C/W °C/W
Package Thermal Resistance, D^2PAK, 5-Pin :	Junction-to-Case, $R_{\theta JC}$ Junction-to-Ambient, $R_{\theta JA}$	- -	TBD TBD	°C/W °C/W
Package Thermal Resistance, TO-220, 5-Lead:	Junction-to-Case, $R_{\theta JC}$ Junction-to-Ambient, $R_{\theta JA}$	- -	TBD TBD	°C/W °C/W
Lead Temperature Soldering	Reflow (SMD styles only) Note 1 Wave Solder (through hole styles only) Note 2	- -	240 Peak (Note 3) 260 Peak	°C °C

1. 10 seconds max.
2. 60 seconds max above 183°C.
3. -5 °C/+0°C allowable conditions.

*The maximum package power dissipation must be observed.

†During the voltage range which exceeds the maximum tested voltage of I, operation is assured, but not specified. Wider limits may apply. Thermal dissipation must be observed closely.

ELECTRICAL CHARACTERISTICS (I = 13.5 V; -40°C < T_J < 150°C; unless otherwise noted)

Characteristic	Test Conditions	Min	Typ	Max	Unit
Output					
Output Voltage, 5.0 V Version	5.0 mA < I_Q < 400 mA, 6.0 V < V_I < 28 V	4.8	5.0	5.2	V
Output Voltage, 5.0 V Version	5.0 mA < I_Q < 200 mA, 6.0 V < V_I < 40 V	4.8	5.0	5.2	V
Output Voltage, 3.3 V Version	5.0 mA < I_Q < 400 mA, 6.0 V < V_I < 28 V	3.168	3.300	3.432	V
Output Voltage, 3.3 V Version	5.0 mA < I_Q < 200 mA, 6.0 V < V_I < 40 V	3.168	3.300	3.432	V
Output Voltage, 2.5 V Version	5.0 mA < I_Q < 400 mA, 6.0 V < V_I < 28 V	2.4	2.5	2.6	V
Output Voltage, 2.5 V Version	5.0 mA < I_Q < 200 mA, 6.0 V < V_I < 40 V	2.4	2.5	2.6	V
Output Voltage, 1.8 V Version	5.0 mA < I_Q < 400 mA, 6.0 V < V_I < 28 V	1.728	1.800	1.872	V
Output Voltage, 1.8 V Version	5.0 mA < I_Q < 200 mA, 6.0 V < V_I < 40 V	1.728	1.800	1.872	V
Output Voltage Tolerance, Adjustable Version	R2 < 50 k, Q + 1.0 V < I < 40 V, I > 4.5 V, 5.0 mA < I_Q < 400 mA	-4.0	-	4.0	%
Output Current Limitation (Note 4)	-	400	600	1100	mA
Output Current Limitation (Sleep Mode) $I_q = I_I - I_Q$	INH = 0 V, T_J < 100°C	-	-	10	μA
Quiescent Current, $I_q = I_I - I_Q$	I_Q = 1.0 mA	-	100	220	μA
Quiescent Current, $I_q = I_I - I_Q$	I_Q = 250 mA	-	5.0	10	mA

ELECTRICAL CHARACTERISTICS (continued) (I = 13.5 V; -40°C < T_J < 150°C; unless otherwise noted)

Characteristic	Test Conditions	Min	Typ	Max	Unit
Output (continued)					
Quiescent Current, $I_q = I_I - I_Q$	I_Q = 400 mA	-	15	25	mA
Dropout Voltage (Note 3), 5.0 V Version 3.3 V Version 2.5 V Version 1.8 V Version	I_Q = 250 mA, $V_{dr} = V_I - V_Q$	 - - - -	 250 - - -	 500 1.2 2.0 2.7	 mV V V V

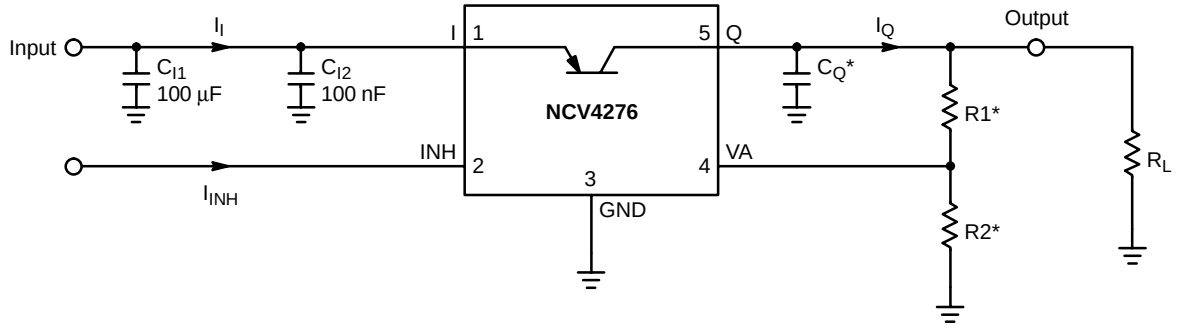
ELECTRICAL CHARACTERISTICS (Continued) (I = 13.5 V; -40°C < T_J < 150°C; unless otherwise noted)

Characteristic	Test Conditions	Min	Typ	Max	Unit
Output					
Dropout Voltage (Note 4), Adjustable Version	I_Q = 250 mA, I > 4.5 V, $V_{dr} = V_I - V_Q$	-	250	500	mV
Load Regulation	I_Q = 5.0 mA to 400 mA	-	5.0	35	mV
Line Regulation	ΔV = 12 V to 32 V, I_Q = 5.0 mA	-	15	25	mV
Power Supply Ripple Rejection	f_r = 100 Hz, V_r = 0.5 V_{pp}	-	54	-	dB
Temperature Output Voltage Drift	-	-	0.5	-	mV/k
Inhibit					
Inhibit On Voltage	Q > 4.9 V	-	2.0	3.5	V
Inhibit Off Voltage	Q < 1.0 V	0.5	1.7	-	V
Input Current	INH = 5.0 V	5.0	10	20	μA

4. Measured when the output voltage V_Q has dropped 100 mV from the nominal value obtained at V_I = 13.5 V.

PIN DESCRIPTION

Pin No.	Symbol	Description
1	I	Input; Battery Supply Input Voltage.
2	INH	Inhibit; Low-active input.
3	GND	Ground; Pin 3 internally connected to heatsink.
4	NC/VA	Not Connected for fixed voltage versions. Voltage Adjust Input; Only for adjustable version. Connect an external voltage driver to set the output voltage.
5	Q	Output; ±4.0%, 400 mA output. Use 22 μF, ESR > 3.0 Ω at 10 kHz to ground.



* 22 μF for Adjustable and 5V Versions.
10 μF for 3.3 V, 2.5 V, and 1.8 V Versions.

Figure 2. Measuring Circuit

Circuit Description

The error amplifier compares a temperature stable reference voltage to a voltage that is proportional to the output voltage (Q) (generated from a resistor divider) and drives the base of a series transistor via a buffer. Saturation control as a function of the load current prevents any oversaturation of the output power device preventing excessive substrate current (quiescent current).

Setting the Output Voltage (Adjustable Version)

The output voltage range of the adjustable version can be set between 2.5 V and 20 V (Figure 4). This is accomplished with an external resistor divider feeding back the voltage to the IC back to the error amplifier by the voltage adjust pin VA. The internal reference voltage is set to a temperature stable reference voltage of 2.5 V.

The output voltage is calculated from the following formula. Ignoring the bias current into the VA pin,

$$Q = [(R1 + R2) * V_{ref}]/R2$$

Use R2 < 50 k to avoid significant output voltage errors due to VA bias current.

Connecting VA directly to Q without R1 and R2 creates an output voltage of 2.5 V.

Designers should consider the tolerance of R1 and R2 during the design phase.

The input voltage range for operation (pin I) of the adjustable version is between (Q + 0.5 V) and 40 V. Internal bias requirements dictate a minimum input voltage of 4.3 V. The dropout voltage for output voltages less than 4 V is (4.3 V - Q).

Calculating Power Dissipation in a Single Output Linear Regulator

The maximum power dissipation for a single output regulator (Figure 3) is:

$$P_{D(max)} = [V_{IN(max)} - V_{OUT(min)}]I_{OUT(max)} + V_{IN(max)}I_q \quad (1)$$

where

$V_{IN(max)}$ is the maximum input voltage,
$V_{OUT(min)}$ is the minimum output voltage,
$I_{OUT(max)}$ is the maximum output current for the application,
I_Q is the quiescent current the regulator consumes at $I_{OUT(max)}$.

Once the value of $P_{D(max)}$ is known, the maximum permissible value of $R_{\Theta JA}$ can be calculated:

$$R_{\Theta JA} = \frac{150^\circ C - T_A}{P_D} \quad (2)$$

The value of $R_{\Theta JA}$ can then be compared with those in the package section of the data sheet. Those packages with $R_{\Theta JA}$'s less than the calculated value in Equation 2 will keep the die temperature below 150°C.

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.

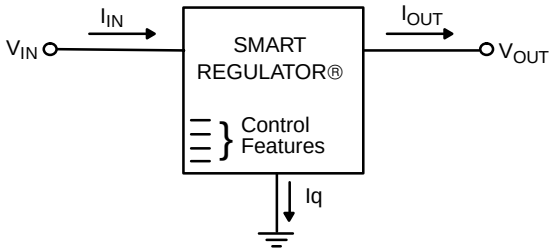


Figure 3. Single Output Regulator with Key Performance Parameters Labeled

Heat Sinks

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{\Theta JA}$:

$$R_{\Theta JA} = R_{\Theta JC} + R_{\Theta CS} + R_{\Theta SA} \quad (3)$$

where

$R_{\Theta JC}$ is the junction-to-case thermal resistance,
$R_{\Theta CS}$ is the case-to-heatsink thermal resistance,
$R_{\Theta SA}$ is the heatsink-to-ambient thermal resistance.

$R_{\Theta JC}$ appears in the package section of the data sheet. Like $R_{\Theta JA}$, it too is a function of package type. $R_{\Theta CS}$ and $R_{\Theta SA}$ are functions of the package type, heatsink and the interface between them. These values appear in heat sink data sheets of heat sink manufacturers.

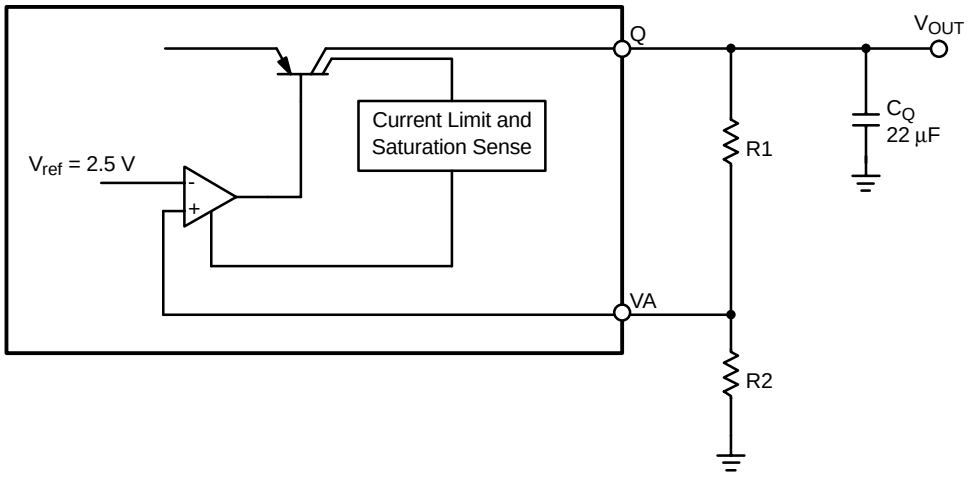
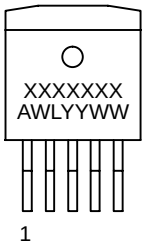


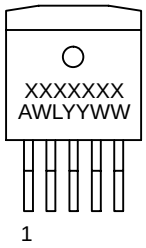
Figure 4. Adjustable Version Application Setup

MARKING DIAGRAMS

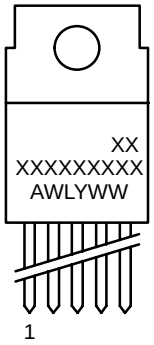
DPAK
DT SUFFIX
CASE TBD



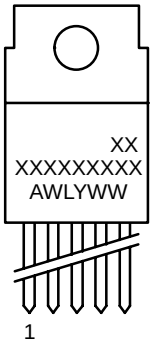
D²PAK
DP SUFFIX
CASE 936A-02



TO-220
TQ SUFFIX
CASE 314D



TO-220
TQVA SUFFIX
CASE 314N



XXX... = Specific Device Code
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

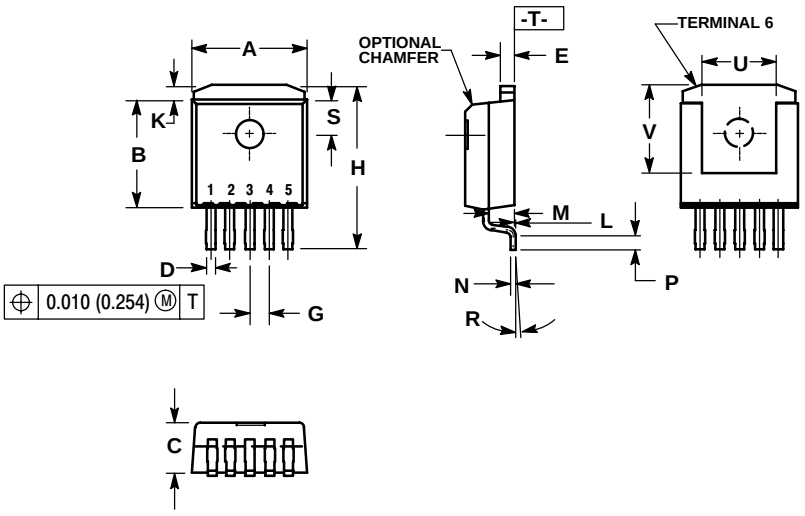
ORDERING INFORMATION

Device	Output Voltage	Package	Shipping
NCV4276DTADJ	Adjustable	DPAK, 5-Pin	xx Units/Rail
NCV4276DTADJRK			xxx Tape & Reel
NCV4276DPADJ		D^2PAK, 5-Pin	50 Units/Rail
NCV4276DPADJR5			750 Tape & Reel
NCV4276TQ5ADJ		TO-220, 5-Lead, Straight	50 Units/Rail
NCV4276TQVA5ADJ		TO-220, 5-Lead, Vertical	50 Units/Rail
NCV4276DT50	5.0 V	DPAK, 5-Pin	xx Units/Rail
NCV4276DT50RK			xxx Tape & Reel
NCV4276DP50		D^2PAK, 5-Pin	50 Units/Rail
NCV4276DP50R5			750 Tape & Reel
NCV4276TQ50		TO-220, 5-Lead, Straight	50 Units/Rail
NCV4276TQVA50		TO-220, 5-Lead, Vertical	50 Units/Rail
NCV4276DT33	3.3 V	DPAK, 5-Pin	xx Units/Rail
NCV4276DT33RK			xxx Tape & Reel
NCV4276DP33		D^2PAK, 5-Pin	50 Units/Rail
NCV4276DP33R5			750 Tape & Reel
NCV4276TQ33		TO-220, 5-Lead, Straight	50 Units/Rail
NCV4276TQVA33		TO-220, 5-Lead, Vertical	50 Units/Rail
NCV4276DT25	2.5 V	DPAK, 5-Pin	xx Units/Rail
NCV4276DT25RK			xxx Tape & Reel
NCV4276DP25		D^2PAK, 5-Pin	50 Units/Rail
NCV4276DP25R5			750 Tape & Reel
NCV4276TQ25		TO-220, 5-Lead, Straight	50 Units/Rail
NCV4276TQVA25		TO-220, 5-Lead, Vertical	50 Units/Rail
NCV4276DT18	1.8 V	DPAK, 5-Pin	xx Units/Rail
NCV4276DT18RK			xxx Tape & Reel
NCV4276DP18		D^2PAK, 5-Pin	50 Units/Rail
NCV4276DP18R5			750 Tape & Reel
NCV4276TQ18		TO-220, 5-Lead, Straight	50 Units/Rail
NCV4276TQVA18		TO-220, 5-Lead, Vertical	50 Units/Rail

PACKAGE DIMENSIONS

DPAK, 5-PIN
DT SUFFIX
CASE TBD
ISSUE TBD

D^2PAK
CASE 936A-02
ISSUE B

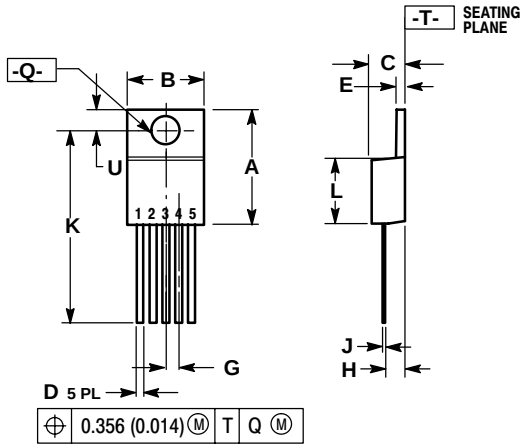


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. TAB CONTOUR OPTIONAL WITHIN DIMENSIONS A AND K.
4. DIMENSIONS U AND V ESTABLISH A MINIMUM MOUNTING SURFACE FOR TERMINAL 6.
5. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS. MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.025 (0.635) MAXIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.386	0.403	9.804	10.236
B	0.356	0.368	9.042	9.347
C	0.170	0.180	4.318	4.572
D	0.026	0.036	0.660	0.914
E	0.045	0.055	1.143	1.397
G	0.067 BSC		1.702 BSC	
H	0.539	0.579	13.691	14.707
K	0.050 REF		1.270 REF	
L	0.000	0.010	0.000	0.254
M	0.088	0.102	2.235	2.591
N	0.018	0.026	0.457	0.660
P	0.058	0.078	1.473	1.981
R	5° REF		5° REF	
S	0.116 REF		2.946 REF	
U	0.200 MIN		5.080 MIN	
V	0.250 MIN		6.350 MIN	

PACKAGE DIMENSIONS

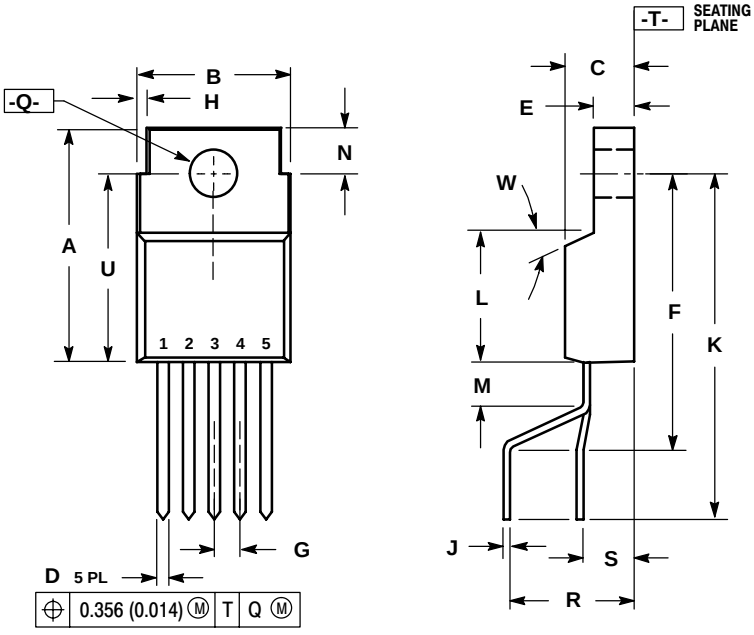
TO-220
FIVE LEAD
T SUFFIX
CASE 314D-04
ISSUE E

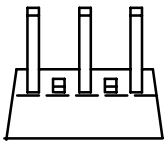


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION D DOES NOT INCLUDE INTERCONNECT BAR (DAMBAR) PROTRUSION. DIMENSION D INCLUDING PROTRUSION SHALL NOT EXCEED 10.92 (0.043) MAXIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.572	0.613	14.529	15.570
B	0.390	0.415	9.906	10.541
C	0.170	0.180	4.318	4.572
D	0.025	0.038	0.635	0.965
E	0.048	0.055	1.219	1.397
G	0.067 BSC		1.702 BSC	
H	0.087	0.112	2.210	2.845
J	0.015	0.025	0.381	0.635
K	0.990	1.045	25.146	26.543
L	0.320	0.365	8.128	9.271
Q	0.140	0.153	3.556	3.886
U	0.105	0.117	2.667	2.972

TO-220
FIVE LEAD
TFVA SUFFIX
CASE 314N-01
ISSUE O





NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION D DOES NOT INCLUDE INTERCONNECT BAR (DAMBAR) PROTRUSION. DIMENSION D INCLUDING PROTRUSION SHALL NOT EXCEED 10.92 (0.043) MAXIMUM.
4. LEADS MAINTAIN A RIGHT ANGLE WITH RESPECT TO THE PACKAGE BODY TO WITHIN ± 0.015 ".

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.604	0.614	15.34	15.60
B	0.395	0.405	10.03	10.29
C	0.175	0.185	4.44	4.70
D	0.027	0.037	0.69	0.94
E	0.100	0.110	2.54	2.79
F	0.712	0.727	18.08	18.47
G	0.067 BSC		1.70 BSC	
H	0.020	0.030	0.51	0.76
J	0.014	0.022	0.36	0.56
K	0.889	0.904	22.58	22.96
L	0.324	0.339	8.23	8.61
M	0.115	0.130	2.92	3.30
N	0.115	0.125	2.92	3.17
Q	0.120	0.130	3.05	3.30
R	0.292	0.342	7.42	8.69
S	0.133	0.183	3.38	4.65
U	0.480	0.495	12.19	12.57
W	5 °		5 °	

Notes

PUBLICATION ORDERING INFORMATION

Literature Fulfillment:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
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Email: ONlit@hibbertco.com

N. American Technical Support: 800-282-9855 Toll Free USA/Canada

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2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051
Phone: 81-3-5773-3850

ON Semiconductor Website: http://onsemi.com

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